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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PIZIALI, JEFFREY J	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 07/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/287,304	YAMAMOTO ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed (on 27 April 2006) in this application after final rejection (mailed 23 January 2006). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on 27 April 2006 has been entered.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. The drawings were received on 21 November 2001. These drawings are acceptable.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. All four independent claims 1 and 14-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Claim 1 recites, "*a plurality of signal lines that are connected to a plurality of data bus lines via analog switches*" (see lines 12-13). Claim 14 recites, "*signal lines in each of said blocks are connected to a plurality of data bus lines via analog switches*" (see lines 13-14). Claim 15 recites, "*divided signal lines in each of said plurality of blocks are connected to a plurality of data bus lines via analog switches*" (see lines 11-13). Claim 16 recites, "*a plurality of signal lines that extend into the liquid crystal display device and are connected to a plurality of data bus lines via analog switches*" (see lines 10-11).

However, the specification contradictorily teaches the horizontal display signal lines [Fig. 7; 74A] being directly connected to the vertical data bus lines [Fig. 7; 68A], and the display panel [Fig. 7; 16] being connected to the data bus lines [Fig. 7; 68A] via analog switches [Fig. 7; 66] (see Page 8, Lines 7-33 of the instant specification). Although only one inventive embodiment (illustrated in Figure 7) is referenced explicitly here, all other pending embodiments are identical as regarding the aforementioned subject matter.

6. The remaining claims 2-13 and 17-21 are rejected under 35 U.S.C. 112, first paragraph, due to their respective dependencies upon rejected base claims.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-6, 8-16, and 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by *Nakajima* (US 5,654,735 A).

Regarding claim 1, Nakajima discloses a liquid crystal display device including a data driver [Fig. 1; 13] and a gate driver [Fig. 1; 12], comprising an LCD panel [Fig. 1; 1] having two opposing flat surfaces, an area of one of the flat surfaces for displaying an image, and at least two edges opposing one another about the flat surfaces and outside of the display area; a substrate on which the LCD panel, the data driver and the gate driver are integrally formed; the data driver on a single edge of the at least two opposing edges of the LCD panel being divided into a plurality of blocks [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.] so as to divide the LCD panel into sections arranged side by side, which simultaneously supply the LCD panel with display signals respectively supplied thereto, wherein each of the blocks includes a plurality of signal lines [Fig. 1; V_n, V_{n+1}, etc.] that are connected to a plurality of data bus lines [Fig. 1; SIG1-SIG3, $Ø_n$, $Ø_{n+1}$, $Ø_{n+2}$, etc.] via analog switches [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.], a number of the data bus lines being larger than a number of the signal lines, the display signals simultaneously being supplied from the plurality of signal lines [Fig. 1; V_n, V_{n+1}, etc.] to one of the plurality of blocks of the panel [Fig. 1; 1] via analog switches [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.] simultaneously with supplying of the display signals to subsequent ones of the plurality of blocks of the panel (wherein display signals SIG1-SIG3 are illustrated in Figure 1 as all being

concurrently connected/supplied to each and every block HSW_n, HSW_{n+1}, HSW_{n+2}, etc.), and the blocks are arranged adjacent to each other along the single edge of the LCD panel, and each block includes a series of different signal lines (see Column 4, Line 1 - Column 5, Line 31).

Regarding claim 2, Nakajima discloses a block comprising a shift register [Fig. 1; 15]; signal lines [Fig. 1; V_n, V_{n+1}, etc.] connected to the signal lines and the LCD panel [Fig. 1; 1]; and analog switches [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}] provided in the data bus lines and controlled by an output signal [Fig. 1; $Ø_n$, $Ø_{n+1}$, $Ø_{n+2}$, etc.] of the shift register thereto (see Column 4, Lines 1-42).

Regarding claim 3, Nakajima discloses a driver device [Fig. 1; 2] which receives display data [Fig. 1; VIDEO] externally supplied and outputs the display signals derived therefrom to the blocks of the data driver (see Column 4, Line 43 - Column 5, Line 7).

Regarding claim 4, Nakajima discloses a plurality of driver devices [Fig. 1; 21+24, 22+25, 23+26] which are respectively associated with a plurality of ones of the blocks, each of the plurality of driver devices receiving display data [Fig. 1; VIDEO, SIG1-SIG3] externally supplied and outputting the display signals derived therefrom to associated blocks of the data driver (see Column 4, Line 43 - Column 5, Line 7).

Regarding claim 5, Nakajima discloses the display signal lines of the associated blocks have parts extending from one of the plurality of driver devices through a space located between the associated blocks (see Fig. 1).

Regarding claim 6, Nakajima discloses a substrate on which the LCD panel, data driver and gate driver are integrally formed (see Fig. 1; Column 4, Lines 1-42).

Regarding claim 8, Nakajima discloses a display signal supply device [Fig. 1, VIDEO] which outputs the display data to the driver device (see Column 4, Line 43 - Column 5, Line 7).

Regarding claim 9, Nakajima discloses the display signal display device is formed on the LCD panel (see Column 4, Lines 1-42).

Regarding claim 10, Nakajima discloses a display signal supply device [Fig. 1, VIDEO] which outputs the display data to the plurality of driver devices (see Column 4, Line 43 - Column 5, Line 7).

Regarding claim 11, Nakajima discloses each of the plurality of blocks supplies the LCD panel with a given number [three, for instance] of display signals at once (Column 5, Lines 8-31).

Regarding claim 12, Nakajima discloses the driver device comprises a shift register [Fig. 1; 3] which outputs a shift signal [Fig. 1; SH1, SH2, SH3], first latch circuits [Fig. 1; 21-23] which latch the display data in response to the shift signal, and second latch circuits [Fig. 1; 24-26] which latch the display data from the first latch circuits in response to a latch enable signal [Fig. 1; SH4] externally supplied [Fig. 1; SYNC] (Column 4, Line 43 - Column 5, Line 31).

Regarding claim 13, Nakajima discloses digital-to-analog converters [Fig. 3, 202] which convert the display data from the second latch circuits into analog signals (Column 7, Line 60 - Column 8, Line 23).

Regarding claim 14, this claim is rejected by the reasoning applied in rejecting claim 1; furthermore, Nakajima discloses a liquid crystal display device including a data driver [Fig. 1; 13] and a gate driver [Fig. 1; 12], comprising an LCD panel [Fig. 1; 1] having two opposing flat surfaces, an area of one of the flat surfaces for displaying an image, and at least two edges opposing one another about the flat surfaces and outside of the display area; and groups of signal lines [Fig. 1; V_n, V_{n+1}, etc.] for carrying display signals, the signal lines within each of the groups being adjacent to each other along a single edge of the at least two opposing edges of the LCD panel, and the data driver being divided into a plurality of adjacently arranged blocks [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.] from which the groups of signal lines extend over corresponding partial areas of the LCD device so that each of the groups of signal lines is associated with a respective one of the blocks of the data driver, wherein the signal lines in each of the blocks are connected to a plurality of data bus lines [Fig. 1; SIG1-SIG3, $Ø_n$, $Ø_{n+1}$, $Ø_{n+2}$, etc.] via analog switches [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.], a number of the data bus lines is larger than a number of the signal lines, and the display signals are simultaneously supplied from the groups of signal lines [Fig. 1; V_n, V_{n+1}, etc.] to one of the plurality of blocks of the panel [Fig. 1; 1] via analog switches [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.] simultaneously with supplying of the display signals to subsequent ones of the plurality of blocks of the panel (wherein display

signalsSIG1-SIG3 are illustrated in Figure 1 as all being concurrently connected/supplied to each and every block HSW_n, HSW_{n+1}, HSW_{n+2}, etc.) (see Column 4, Line 1 - Column 5, Line 31).

Regarding claim 15, Nakajima discloses a liquid crystal display device including a data driver [Fig. 1; 13] and a gate driver [Fig. 1; 12], comprising an LCD panel [Fig. 1; 1] having two opposing flat surfaces, an area of one of the flat surfaces for displaying an image, and at least two edges opposing one another about the flat surfaces and outside of the display area; signal lines [Fig. 1; V_n, V_{n+1}, etc.] extending from the data driver and carrying display signals, the data driver and the signal lines being divided into a plurality of blocks [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.] so that the divided signal lines extending from one of the plurality of blocks extends over a corresponding divided area of the LCD device; wherein the plurality of blocks are adjacent to each other along a single edge of the at least two opposing edges of the LCD panel, the divided signal lines in each of the plurality of blocks are connected to a plurality of data bus lines [Fig. 1; SIG1-SIG3, $Ø_n$, $Ø_{n+1}$, $Ø_{n+2}$, etc.] via analog switches [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.], a number of the data bus lines being larger than a number of the signal lines, and display signals being simultaneously supplied from the plurality of signal lines [Fig. 1; V_n, V_{n+1}, etc.] to one of the plurality of blocks of the panel [Fig. 1; 1] via analog switches [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.] simultaneously with supplying of the display signals to subsequent ones of the plurality of blocks of the panel (wherein display signals SIG1-SIG3 are illustrated in Figure 1 as all being concurrently connected/supplied to each and every block HSW_n, HSW_{n+1}, HSW_{n+2}, etc.) (see Column 4, Line 1 - Column 5, Line 31).

Regarding claim 16, Nakajima discloses a liquid crystal display device including a data driver [Fig. 1; 13] and a gate driver [Fig. 1; 12], comprising an LCD panel [Fig. 1; 1] having two opposing flat surfaces, an area of one of the flat surfaces for displaying an image, and at least two edges opposing one another about the flat surfaces and outside of the display area; a substrate on which the LCD panel, the data driver and the gate driver are integrally formed; the data driver being divided into a plurality of blocks [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.] arranged side by side along a single edge of the at least two opposing edges of the LCD panel, and each of the blocks has a plurality of signal lines [Fig. 1; V_n, V_{n+1}, etc.] that extend into the liquid crystal display device and are connected to a plurality of data bus lines [Fig. 1; SIG1-SIG3, $Ø_n$, $Ø_{n+1}$, $Ø_{n+2}$, etc.] via analog switches [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.], a number of the data bus lines being larger than a number of the signal lines, and display signals being simultaneously supplied from the plurality of signal lines [Fig. 1; V_n, V_{n+1}, etc.] to one of the plurality of blocks of the panel [Fig. 1; 1] via analog switches [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.] simultaneously with supplying of the display signals to subsequent ones of the plurality of blocks of the panel (wherein display signals SIG1-SIG3 are illustrated in Figure 1 as all being concurrently connected/supplied to each and every block HSW_n, HSW_{n+1}, HSW_{n+2}, etc.) (see Column 4, Line 1 - Column 5, Line 31).

Regarding claim 18, Nakajima discloses each of the blocks [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.] is arranged adjacent to a block of at least one of an immediately preceding block and an immediately following block (see Fig. 1).

Regarding claim 19, this claim is rejected by the reasoning applied in the above rejection of claim 18.

Regarding claim 20, this claim is rejected by the reasoning applied in the above rejection of claim 18.

Regarding claim 21, this claim is rejected by the reasoning applied in the above rejection of claim 18.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 7 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Nakajima* (US 5,654,735) in view of *Lewis* (US 6,040,812 A).

Regarding claims 7 and 17, Nakajima discloses the use of thin film transistors (see Column 4, Lines 6-7). Yet, Nakajima does not expressly teach the data driver comprising polysilicon transistors.

However, Lewis does disclose, "Polysilicon thin film transistors (poly-Si TFTs), for example, can be used as switching elements in an active matrix array and can also be used in drive circuitry integrated on the same substrate as the array" (see Column 1, Lines 54-63).

Nakajima and Lewis are analogous art, because they are from the shared field of driving display arrays. Therefore, it would have been obvious to one skilled in the art at the time of invention to use Lewis' polysilicon transistors within Nakajima's data driver, so as to make it more easily possible to integrate an active matrix array for a display on the same substrate with its drive circuitry (see Lewis: Column 1, Lines 54-63).

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Response to Arguments

12. Applicants' arguments filed 27 April 2006 have been fully considered but they are not persuasive.

The applicants allege, "*the Examiner is attempting to restrict the data bus lines 68A to being only those portions of the data lines between the switch units 66 and the signal lines 64. Nothing in Fig. 7 however, or its accompanying text, so unreasonably limits the interpretation of what constitutes a 'data bus line' in the present Application. The examiner's interpretation of Fig. 7 therefore, is without support from the present Application*" (see Page 10 of the 'Amendment M' filed 27 April 2006). However, the examiner respectfully disputes the

applicants' allegation of impropriety. The instant Specification itself limits what constitutes a "*data bus line*" to [Figs. 1 & 3; 22] (see Page 1; Lines 20-35) and [Fig. 7; 68A] (see Page 8, Lines 7-33).

The applicants state, "*For the Examiner's interpretation to have any merit otherwise, the Examiner must have demonstrated that one of ordinary skill in the art would presume that a 'data bus line' would constitute only that portion of the bus line outside of the boundaries of the display panel 16, and none of the portion of the lines that extend into the display panel, and its individual display elements*" (see Page 10 of the 'Amendment M' filed 27 April 2006). The rejection under 35 U.S.C. 112, first paragraph "has merit," because the instant Specification defines what constitutes a "*data bus line*" in direct contradiction to what is presently being claimed. The instant Specification does not acknowledge the existence of any "data bus lines" extending into the display panel, and its individual display elements (as now alleged by the applicants). The absence of such subject matter is not a *misinterpretation*, it is a fact.

The applicants next contend, "*The proper standard of review was to determine what one of ordinary skill in the art would understand when interpreting the claims in light of the Specification*" (see Page 10 of the 'Amendment M' filed 27 April 2006). Actually however, the examiner respectfully counters that the "*proper standard of review*" is to determine whether or not the Specification contains a written description of the invention, and of the manner and process of making and using it, in such ***full, clear, concise, and exact terms*** as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same.

The applicants defend the subject matter contradiction between the Specification and the Claims, not by pointing to any particular teaching(s) within the Specification, but by arguing,

"*One skilled in the art, however, is well apprised that data bus lines are commonly known to be the bus lines that actually extend into and through the display panel, and even are capable of connecting to each individual display element in the panel*" (see Pages 10-11 of the 'Amendment M' filed 27 April 2006). So instead of interpreting the claims in light of the Specification, the applicants expect that one of ordinary skill in the art would just somehow get the general gist of what the claimed subject matter means. Unfortunately, this "commonly known" defense hardly qualifies as a "***full, clear, concise, and exact***" written description.

Next the applicants accuse the examiner of neglecting to "*answer the meritorious arguments presented by Applicants traversing the [previous] rejection*" (see Page 11 of the 'Amendment M' filed 27 April 2006). The applicants don't go on any further to explain what exact "*meritorious arguments*" where supposedly ignored by the examiner, or whether the examiner incidentally answered only non-meritorious arguments. Accordingly, the examiner will simply address all the currently presented arguments (found within the 'Amendment M' filed 27 April 2006).

The applicants contend, "*In his 'Response to Arguments,' [mailed 23 January 2006] the examiner improperly relies upon what he asserts to be 'inherent' results of the structure described in the present Specification. It is improper for the Examiner, however, to base an anticipation of obviousness rejection upon the teachings of the present Specification*" (see Pages 11-12 of the 'Amendment M' filed 27 April 2006). The applicants are respectfully reminded that "*inherent results*" have more to do with the laws of nature rather than any particular hindsight teachings within the present Specification.

According to the 'Amendment M' filed 27 April 2006, "*Applicants specifically traverse the Examiner's assertion that the simultaneous transmission features of the present invention 'appear to be little more than the inherent result of the signal lines... and the data bus lines... being connected to one another.' Nothing in the cited portion of the present Specification (page 8, lines 7-33) describes that these claim features are an 'inherent result'*" (see Page 12 of the 'Amendment M' filed 27 April 2006). Respectfully, it would seem from the above two quotes that the applicants find allegations of "*inherent subject matter*" based on the teachings of the present Specification equally improper as allegations of "*inherent subject matter*" not based on the teachings of the present Specification.

The applicants next state, "*Anticipation and obviousness must be based upon the teachings and suggestions of the prior art, and may not be based on the teachings of the present Specification. Use of the present Specification in this way demonstrates an impermissible use of hindsight. For at least these reasons as well, the rejections must be withdrawn*" (see Page 12 of the 'Amendment M' filed 27 April 2006). Again, the applicants appear to be uncertain in their denouncements of the Office Action (mailed 23 January 2006) whether the included rejections do or don't rely upon teachings of the present Specification. Since the applicants have neglected to point to any particular hindsight applications by the examiner, it is rendered rather difficult to respond to the applicants' insinuations of impropriety here.

Despite the fact that all but two claims were and are rejected under 35 U.S.C. 102(b), in response to applicants' argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed

invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

The applicants also contend, "*the Examiner incorrectly asserts that 'it could be said that Nakajima teaches 'two-way transmission' between those same signal lines and data bus lines'*" (see Page 12 of the 'Amendment M' filed 27 April 2006). In response to applicants' argument that the references fail to show certain features of applicants' invention, it is noted that the features upon which applicant relies (i.e., "*two-way transmission*") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The applicants next state, "*Applicants further note for the record that the Examiner has not remarked upon or answered the many meritorious arguments presented by Applicants that describe how the Nakajima reference itself teaches away from the present invention. All of the transmitted signals that the Examiner asserts to be 'simultaneous' in the Nakajima reference are never actually described by Nakajima to be simultaneously transmitted. Because the Examiner has not rebutted these arguments, the rejection must still further be withdrawn*" (see Page 13 of the 'Amendment M' filed 27 April 2006). Looking back at page 11 (Paragraphs 2 & 3) of the Office Action mailed 23 January 2006, it certainly does appear that this examiner did in fact previously rebut arguments about "*simultaneously transmitted signal*" subject matter. The

applicants are respectfully reminded that just because they disagree with the examiner's rebuttal, it does not follow that the rebuttal is altogether nonexistent.

Lastly, the applicants argue, "*the portions of Nakajima cited by the Examiner teach only the simultaneous sampling of the video signals (col. 4, lines 22-23 and 30-31, for example), but not that such signals are also simultaneously transmitted, as featured in the present invention. In fact, Nakajima even teaches away from such features, and the Examiner has not cited to any teachings or suggestions within the reference that dispute this fact. Nakajima expressly teaches that the sampled video signals SIG1-SIG3 are sequentially output to the blocks shown in Fig. 1. Fig. 2 of Nakajima unequivocally illustrates that the signal Vn applied to the block corresponding to element HSWn occurs sequentially prior to the signal Vn+1 being applied to the subsequent block corresponding to element HSWn+1. None of the signals applied to the subsequent blocks are ever described or shown to occur simultaneously*" (see Page 14 of the 'Amendment M' filed 27 April 2006). However, the examiner respectfully disagrees.

Nakajima clearly discloses that each sampled video signal line [Fig. 1; SIG1, SIG2, and SIG3] is concurrently shared by and connected to each block [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.]. That is to say, when a signal is applied to a line [Fig. 1; SIG1, for instance], that signal will be simultaneously transmitted to each and every block [Fig. 1; HSW_n, HSW_{n+1}, HSW_{n+2}, etc.] (see Column 4, Lines 1-42).

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

The applicants are hereby notified that the examiner's art unit has recently changed from Art Unit 2673 to Art Unit 2629, please direct all future correspondence accordingly. Thank you.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

J.P.
6 July 2006